DAY 1:

Simulator tool used: iverilog

Waveforms viewed in Gtkwave

Synthesizer used: yosys

A screenshot of a computer

AI-generated content may be incorrect.

VCD file created by passing RTL design and testbench to iverilog

A screenshot of a computer

AI-generated content may be incorrect.

Gtkwave simulation waveform

A screenshot of a computer

AI-generated content may be incorrect.

Synthesizing design using yosys and linking to standard library cells

A screenshot of a computer

AI-generated content may be incorrect.

Synthesized 2:1 mux design after which a netlist was created.